Claims Appendix
(Showing Support for Claims)

1. A memory controller ([0084]; FIG. 1, 100), comprising:

a memory ([0087] & [0095], discussing "memory map 1100" and "MAR 1102"; FIG. 11) to store indications of data/strobe ratios ([0087]) that are required to access memory devices ([0083]), discussing "memory modules" and "RAM devices") that are coupled to the memory controller, said memory being addressed during memory device accesses of said memory controller;

subsets of strobe drivers ([0085], [0086], [0094]), wherein each of said subsets receives addressed indications of data/strobe ratios during write cycles of the memory controller, and wherein at least one of said subsets generates strobes in response to only some of said indications of data/strobe ratios;

pluralities of strobe receivers and data receivers ([0184], [0185], [0186]; FIGS. 10 & 18); and

a switching network ([0184], discussing "multiplexer 1812") to associate at least some of said strobe receivers with at least some of said data receivers, wherein said switching network receives addressed indications of data/strobe ratios during read cycles of the memory controller, and wherein said switching network associates different ones of said strobe receivers with said data receivers in response to different indications of data/strobe ratios.

2. The memory controller of claim 1, wherein each of said indications of a data/strobe ratio is stored in said memory as a single bit ([0088]), and is addressed by a designator of a particular one of said memory devices ([0093]; FIG. 11).

3. The memory controller of claim 1, wherein the memory controller is a DDR memory controller ([0084]).

4. The memory controller of claim 1, wherein said indications of data/strobe ratios are used to configure said drivers and receivers for source synchronous accesses of the memory devices ([0005], [0038], [0075], [0139]).

5. The memory controller of claim 1, wherein said memory devices are DDR memory devices ([0084]; 104a, 104b, FIG. 9).

6. The memory controller of claim 1, wherein:

said data receivers comprise storage elements ([0183], discussing "data latches 1802-1808"; FIG. 18) to receive data from said memory devices;

said strobe receivers comprise counters ([0136], [0185]; 1900, FIG. 19) for producing counts of strobe edges received from said memory devices; and

said switching network comprises:

i) control inputs ([0186]; set_alt_n, FIG. 18) which are responsive to said addressed indications of data/strobe ratios;

ii) a plurality of data inputs ([0136], [0185]; S1 – S4, S1_alt – S4_alt, FIG. 18) which receive plural ones of said counts; and

iii) a plurality of outputs ([00186]; output of multiplexer 1812, FIG. 18), each coupled to control the storage elements of those data receivers associated with one of said strobe receivers.

7. The memory controller of claim 1, wherein the switching network comprises a number of multiplexers (1812, FIG. 18) to associate the strobe receivers with the data receivers.

8. The memory controller of claim 1, wherein said indications of data/strobe ratios are derived from a serial presence detect ([0091]) that is executed by the memory controller.

9. A memory controller ([0084]; FIG. 1, 100), comprising:

a memory ([0087] & [0095], discussing "memory map 1100" and "MAR 1102"; FIG. 11) to store indications of data/strobe ratios ([0087]) that are required to access memory devices ([0083]) that are required to access memory devices ([0083]), discussing "memory modules" and "RAM devices") that are coupled to the memory controller; and

a memory interface ([0084]; memory interface 900, FIG. 9) through which the memory controller initiates data transmissions with the memory devices; wherein, for a data transmission initiated with a particular one of the memory devices, the ratio of data signals to strobe signals sent/received through the interface is dynamically determined in response to a corresponding indication of a data/strobe ratio stored in the memory.

10. The memory controller of claim 9, wherein the memory is addressed during data transmissions of the memory controller; the memory controller further comprising:

a plurality of data pads ([0085]; pads DQ0-DQ7, FIG. 9);

a plurality of strobe pads ([0085]; pads DQS0, DQS18, FIG. 9);

strobe driver circuitry ([0085], [0086], [0094]) to, during a write to a particular memory device, generate strobes at a subset of said strobe pads determined by a corresponding indication of a data/strobe ratio stored in the memory; and

control circuitry ([0184], [0185], [0186]; FIGS. 10 & 18) to, during a read from a particular memory device, controlling data receipt at a subset of said data pads in response to strobes received at a subset of said strobe pads, wherein said subset of strobe pads is determined by a corresponding indication of a data/strobe ratio stored in the memory.

11. The memory controller of claim 10, wherein the memory is addressed during each data transmission of the memory controller ([0093]).

12. The memory controller of claim 9, wherein each of said stored indications of data/strobe ratios is stored in said memory as a single bit ([0088]), and is addressed by a designator of a particular one of the memory devices ([0093]; FIG. 11).

13. The memory controller of claim 9, wherein the memory controller is a DDR memory controller ([0084]), and wherein each of said bits stored in the memory has two values corresponding, respectively, to 4:1 and 8:1 data/strobe ratios ([0088]).

14. The memory controller of claim 9, wherein the indications of data/strobe ratios stored in the memory correspond to at least x4, x8 and x16 DDR SDRAMs ([0089]).

15. The memory controller of claim 9, wherein the indications of data/strobe ratios stored in the memory are RAM device data widths of the memory devices ([0090]).

16. The memory controller of claim 15, wherein said RAM device data widths are DDR SDRAM device data widths ([0090]).

17. A memory controller ([0084]; FIG. 1, 100), comprising:

a plurality of data pads ([0085]; pads DQ0-DQ7, FIG. 9);

a plurality of strobe pads ([0085]; pads DQS0, DQS18, FIG. 9);

means ([0091], e.g., serial presence detect) for reading a data width from each of a number of memory devices coupled to said memory controller; and

means ([0095], [0096], discussing "MAR 1102" and circuitry receiving "act_stb[0]" and :act_stb[1]"; FIGS. 8, 9 & 12; [0184], discussing "multiplexer 1812"; FIG. 18) for associating ones of said strobe pads with ones of said data pads when communicating with said memory devices, in one or more of a plurality of data/strobe ratios supported by the memory controller, and in

data/strobe ratio(s) determined by said data width(s) read from said number of memory devices.

18. The memory controller of claim 17, further comprising means ([0087] & [0095], discussing "memory map 1100" and "MAR 1102"; FIG. 11) for storing indications of said data widths read from the number of memory devices; wherein, each time the memory controller communicates with a particular memory device, said associating means addresses the memory to determine a data/strobe ratio of the memory device.

19. The memory controller of claim 18, wherein said storing means is a memory map (memory map 1100, FIG. 11).

20. The memory controller of claim 17, wherein said means for reading a data width from each of the number of memory devices comprises means for executing a serial presence detect sequence within the memory devices ([0091]).